WHAT IS CLAIMED IS:

1. A memory device comprising:

a matrix of a plurality of memory cells, each of which is connected to an intersection of each bit line of a plurality of pairs of bit lines and each word line of a plurality of word lines which intersect the bit lines;

a plurality of sense amplifiers capable of read and write operations independently of one another, which are disconnectedly connected in parallel with the plurality of memory cells connected to the pairs of bit lines, through the pairs of bit lines; and

a read gate and a write gate which are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines,

wherein the memory device is controlled so that read data is read out successively, when a word line to be activated, of the plurality of word lines is switched to another word line to be activated.

2. The memory device according to claim 1 comprising a plurality of read gates and a plurality of write gates which are separately connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

3. The memory device according to claim 1 comprising a common read gate and a common write gate which are connected to each of the plurality of sense amplifiers connected in parallel with the pairs of bit lines.

4. The memory device according to claim 1, wherein each

of the plurality of memory cells comprises a dynamic RAM.

5. The memory device according to claim 2, wherein each of the plurality of memory cells comprises a dynamic RAM.

6. The memory device according to claim 3, wherein each of the plurality of memory cells comprises a dynamic RAM.